REMARKS

Claims 1, 4, 6-11, 13-17, 19, 21-23 and 25-28 are pending in this application. By this Amendment, claims 2-3, 5, 12, 18, 20 and 24 are cancelled. Applicant has attached replacement drawing sheets for Figs. 8, 10 and 12 to correct a minor error in the original drawings. Specifically, these figures are amended to clarify that output of the AND gate is supplied to 8 pixels. Reconsideration in view of the foregoing amendments and following Remarks is respectfully requested.

The Office Action rejects claim 1 under 35 U.S.C. §102(e) over U.S. Patent No. 6,452,637 to Umeda et al. and rejects claims 2-3 and 6 under 35 U.S.C. §102(e) over U.S. Patent No. 6,549,234 to Lee. Applicant respectfully traverses the rejection.

Regarding claim 1, Applicant submits that neither Umeda et al. nor Lee discloses or suggests a CMOS image sensor comprising pixel sensors arranged in the form of a two dimensional array, each pixel sensor comprising a photo diode at a signal detection node and a pair of pass transistors, which passes a photo diode reset signal to a gate of a transistor that resets the photo diode only when the pixel sensor is selected, means in each pixel sensor for obtaining a signal whose reset noise is reduced and that corresponds to the absolute value of the amount of incident light, and means for outputting the signal in a block scanning fashion, wherein the photo diode reset signal is given as the logical AND of a column block selection signal and a pixel reset signal, as recited in amended claim 1. Claim 1 has been amended to incorporate the subject matter of cancelled claims 2 and 3. Thus, the rejection of claim 1 over Umeda et al. has been rendered moot.

Lee teaches a pixel structure with an electronic shutter function. In Lee, when the line reset signal LRS and the column rest signal CRS are enabled simultaneously, the charge due to photo electrons accumulated in a photo diode is discharged. However, Lee fails to teach means for obtaining a signal whose reset noise is reduced and that corresponds to the absolute

value of the amount of incident light, including means for outputting the signal in a block scanning fashion wherein the photo diode reset signal is given as the logical AND of the column block selection signal and a pixel reset signal.

Regarding claim 6, Applicant respectfully submits that Lee fails to disclose or suggest a CMOS image sensor comprising a <u>plurality of photo gate type pixel sensors</u> arranged in a two dimensional array, a pair of pass transistors for passing a photo gate control signal thereby transferring corresponding signal charges only when a corresponding row is selected, and a pair of pass transistors for passing a pixel transfer signal thereby allowing corresponding signal charges to be transferred only when a corresponding column block is selected, as recited in claim 6.

Like Umeda et al., Lee discloses a photo diode type pixel sensor rather than the photo gate type pixel sensor of claim 6. Also, neither reference discloses that the signal charges of multiple pixel sensors constituting a column block are transferred simultaneously by selecting the corresponding column block. Thus, in view of these distinctions, it is respectfully submitted that claims 1 and 6 are patentable over either Lee or Umeda et al. Accordingly, Applicant respectfully requests that the rejection of claims 1 and 6 be withdrawn.

The Office Action rejects claims 4, 5 and 7 under 35 U.S.C. §103(a) over Lee in view of U.S. Patent No. 6,326,230 to Pain et al. Claim 4 has been amended to incorporate the subject matter of claim 5 and claim 5 has been cancelled. Thus, the rejection of claims 4 and 7 is respectfully traversed.

As discussed above in the context of claim 1, Applicant respectfully submits that Lee does not disclose or suggest a CMOS image sensor comprising means for outputting a signal in block scanning fashion wherein the transfer signal is given as the logical AND of a column block selection signal and a pixel transfer signal. Lee teaches a photo diode type pixel sensor rather than a plurality of photo-gate type pixel sensors. The Office Action alleges that Lee

discloses that the transfer signal is given as the logical AND of a column block selection signal and pixel transfer signal. However, Lee does not disclose a pixel transfer signal as recited in claim 4 and does not disclose that the transfer signal is given as the logical AND of a column block selection signal which selects multiple pixel sensors and a pixel reset signal. Rather, Lee discloses a reset signal, and also discloses that a photo diode is reset by a line reset signal and a column reset signal.

Pain et al. is relied upon in the Office Action as evidence that one of ordinary skill in the art would be motivated to use floating diffusion to temporarily store charges from the photo active region to prevent any loss of image information. However, Applicant respectfully submits that Pain et al. does not make up for the deficiencies of Lee as discussed above. Therefore, Applicant respectfully submits that claims 4 and 7 are patentable over the combination of Lee and Pain et al. Accordingly, Applicant respectfully requests that the rejection of claims 4 and 7 under 35 U.S.C. §103(a) be withdrawn.

The Office Action rejects claims 11, 17 and 23 under 35 U.S.C. §103(a) over Umeda et al. in view of U.S. Patent No. 5,128,769 to Arai et al.; rejects claims 8 and 10 under 35 U.S.C. §103(a) over Lee in view of Umeda et al.; rejects claims 12, 14, 18, 20, 24 and 26 under 35 U.S.C. §103(a) over Lee in view of Arai et al.; rejects claims 16, 22 and 28 under 35 U.S.C. §103(a) over Lee in view of Umeda et al. and further in view of Arai et al.; rejects claim 9 under 35 U.S.C. §103(a) over Lee in view of Pain et al. and further in view of Umeda et al.; and rejects claims 13, 15, 19, 21, 25 and 27 under 35 U.S.C. §103(a) over Lee in view of Pain et al. and further in view of Pain et al. Applicant respectfully traverses the rejection.

The rejection of claims 12, 18, 20 and 24 have been rendered moot by the cancellation of these claims. However, as the rejections apply to the remaining claims they are respectfully traversed. In particular, Applicant respectfully submits that Arai et al. fails to supply the deficiencies of either Umeda et al., Lee or Pain et al. as discussed above in the

Application No. 09/515,504

context of independent claims 1, 4 and 6. Accordingly, Applicant respectfully requests that the rejection of the claims under 35 U.S.C. §103(a) be withdrawn.

Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff Registration No. 27,075

Phillip D. Mancini Registration No. 46,743

JAO:PDM/ccs

Attachments:

Replacement Drawing Sheets

Date: December 22, 2003

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320 Telephone: (703) 836-6400 DEPOSIT ACCOUNT USE
AUTHORIZATION
Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461